REMARKS

This is in full and timely response to the Office Action mailed on January 4, 2005. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 3 and 6-32 are currently pending in this application, with claims 3, 6 and 22 being independent. *No new matter has been added.*

Entry of amendment

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal. Accordingly, entry of this amendment is respectfully requested.

Prematureness

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office action, respectfully requests reconsideration of the finality of the Office action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

Specification objections

The Office Action requests amendments to the Abstract.

While not conceding the propriety of this objection and in order to advance the prosecution of the above-identified application, the Abstract has been amended in the manner requested by the Examiner.

Withdrawal of this objection is respectfully requested.

The following objection is not the subject for the appeal, but a discussion of the objection is provided only for the purposes of completeness.

The Final Office Action includes an objection to the specification as lacking an enabling description, in reference to the limitation "the set information" recited in the independent claim 3.

In response to this contention, please note that section 112 requires only an objective enablement; the invention needs to be sufficiently disclosed through illustrative examples or terminology to teach those of ordinary skill in the art how to make and how to use the invention as broadly as it is claimed. *In re Marzocchi*, 439 F.2d 220, 223, 169 USPQ 367, 369 (CCPA 1971). See also M.P.E.P §§2164.01, 2164.04.

"A specification disclosure which contains a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented ***must*** be taken as in compliance with the enabling requirement of the first paragraph of Section 112 unless there is reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support" (emphasis added). *Fiers v. Revel,* 984 F.2d 1164, 1172, 25 USPQ2d 1601, 1607 (Fed. Cir. 1993). See also M.P.E.P. §2164.04.

Assuming that sufficient reason for such doubt does exist, a rejection for failure to teach how to make and/or use will be proper on that basis; *such a rejection **can be overcome** by suitable proofs indicating that the teaching contained in the specification is truly enabling*. *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (1971).

"*How the specification accomplishes this is not material*. It is not necessary that the application describe the claim limitations exactly, but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that the [Applicant] invented [the claimed invention] (emphasis added). *In re Wertheim,* 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976). "The applicant does not have to utilize any particular form of disclosure to describe the subject matter claimed." *In re Alton*, 76 F.3d 1168, 1172, 37 USPQ2d 1578, 1581 (Fed. Cir. 1996).

The term "the set information" is fully supported within the specification as originally filed. For example:

> The specification as originally filed at page 9, lines 16-20, provides that "as the control means 110 controls the timings to generate both the timing signal and the address specifying signal in conformity with *the set information*, the test pattern cycle period for any address can be varied."
>
> The specification as originally filed at page 9, lines 20-22, provides that "*the set information* is transferred to the semiconductor testing apparatus 100 prior to or during the test by some method."
>
> The specification as originally filed at page 9, lines 23 to page 10, line 2, provides that "in execution of the test, the control means 110 always refers to the latest *set information* to thereby control the timings to generate the timing signal and the address specifying signal."
>
> The specification as originally filed at page 11, lines 13-16, provides that "and *set information* for controlling the cycle period to execute the test pattern of each address is also set prior to start of the test."
>
> The specification as originally filed at page 11, lines 17-22, provides that "upon start of the test, the control means 110 forms an operation reference signal to operate the test pattern, and generates a timing signal to produce a test pattern signal in conformity with *the set information*, and further generates an address specifying signal per cycle period for the test pattern memory means 130."
>
> The specification as originally filed at page 12, lines 17-21, provides that "in this manner, as the control means 110 controls the timings to generate the timing signal and the address specifying signal in conformity with *the set information*, it becomes possible to freely set the test pattern cycle period of any desired address."
>
> The specification as originally filed at page 13, lines 12-18, provides that "in this case, the cycle period rate of the entire test pattern is set to a value (RATE 1) lower

than the maximum operation frequency and, in conformity with *the set information*, the rate of the specific subject address only, i.e., the (N+3)-th cycle, is raised to a higher value (RATE 2)."

The specification as originally filed at page 13, line 24 to page 14, line 3, provides that "and the cycle frequency rate of the specific address can be successively narrowed by changing *the set information*, hence realizing confirmation of the maximum operation frequency in the relevant portion."

The specification as originally filed at page 19, line 19 to page 20, line 1, provides that "in the semiconductor testing apparatus of the present invention, as described hereinabove, a test pattern for a specified address is outputted at a timing corresponding to *set information*, in such a manner that the test pattern is supplied to the semiconductor device, which is being tested, at the timing that conforms with the predetermined *set information*, whereby a test pattern signal is generated on the basis of such test pattern."

The specification as originally filed at page 20, lines 1-4, provides that "as a result, the timing to generate the test pattern of the desired address is controlled in conformity with *the set information*, hence generating a desired test period."

The Office Action contends that the specification lacks an enabling description with respect to the term "the set information" found within the claims (Office Action at page 4). The Office Action further contends that even though numerous examples have been cited, "the set information" is not defined either in the specification or by the Applicant's arguments (Office Action at page 7).

In response, *it is incumbent upon the Patent Office*, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and *to **back up** assertions of its own with acceptable evidence or reasoning* which is inconsistent with the contested statement. *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (1971).

At least for the reasons provided hereinabove, the specification complies with the enablement requirement of 35 U.S.C. §112, first paragraph.

Withdrawal of this objection and allowance of the claims is respectfully requested.

Claim objections

Claims 3 and 6-21 were rejected for the use of the term "adapted to".

This objection is traversed at least for the following reasons.

The term "adapted to" has been previously found by the Examiner to be acceptable claim language. For example, the Examiner has found such claim language acceptable within claims 13 and 15 of U.S. Patent No. 6,809,528. The Examiner has found such claim language acceptable within claim 1 of U.S. Patent No. 6,791,339. The Examiner has also found such claim language acceptable within claim 29 of U.S. Patent No. 6,756,789. Many other examples of the Examiner finding the term "adapted to" as acceptable claim language are within the U.S. Patent collection. Respectfully, this objection is inconsistent with other actions taken by the Examiner. Clarification as to why the term "adapted to" is now deemed unacceptable is respectfully requested.

Withdrawal of this objection and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: March 30, 2005

Respectfully submitted,

By_____

Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant

Attachments Abstract

AMENDMENTS TO THE ABSTRACT

Please substitute the following paragraph(s) for the abstract now appearing in the currently filed specification:

-- The semiconductor testing apparatus includes test pattern memory ~~means~~ adapted for storing and managing test pattern data in accordance with addresses, and outputting the test pattern specified by the desired address; test pattern generator ~~ion means~~ for generating a test pattern signal on the basis of the test pattern outputted from the memory means; and controller ~~means~~ for controlling the test pattern memory ~~means~~ and the test pattern generator ~~ion means~~ in such a manner that the test pattern signal based on the test pattern data of the desired address can be generated at a predetermined timing conforming with the set information. --